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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/738,322	12/16/2003	Richard M. Fastow	AMD-H0563	7930

7590 02/09/2006

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EXAMINER	
WOJCIECHOWICZ, EDWARD JOSEPH	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/738,322	FASTOW ET AL.	
	Examiner	Art Unit	
	Edward Wojciechowicz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-7 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi in view of Wen, Rodgers and Saitoh, all of record. As stated in the previous rejection, the Hayashi reference teaches the basic structure of the claimed invention with the formation of bit lines that are enclosed within and surrounded by the substrate, while Wen, Rodgers and Saitoh teach additional features of the claimed device that are well known in the art, and would be properly combinable with Hayashi.

The primary issue in dispute concerns the proper interpretation of such terms as "buried within", "enclosed within" and "surrounded by" as used in the claims, and within the context of the semiconductor memory cell art.

Applicants', in their remarks accompanying the last amendment, argue that: "there is no definition of the word 'surrounding' which permits Hayashi to be interpreted as reading on Claim 1", and they imply by this argument that the word "surrounding" requires that the bit line be surrounded by the substrate at every point in three dimensional space. However, as commonly used in the semiconductor art, terms such as "surrounding" are typically given a much broader interpretation then that put forth by applicants. For example, surface regions, such as source or drain regions in a field effect transistor, are generally considered to be "surrounded by" the substrate in a lateral sense, even though no part of the substrate is formed above the source or drain region in the vertical plane. Similarly, the semiconductor art is replete with examples of diffused regions in the shape of a ring, which are described as "surrounding" another portion of the substrate. Indeed, the art of record provides just such an example, as seen in FIG. 2 of Rodgers, and discussed in col. 4, l. 31, where ring region (49) is described as "surrounding" the V-shaped

recess, even though, clearly, this ring region is not formed above or below the V-shaped recess. This teaching refutes applicants' argument that: "there is no definition of the word 'surrounding' which permits Hayashi to be interpreted as reading on Claim 1."

Another example of how these terms are typically defined in the art is found in Hayashi's description of the bit lines (6) and (7) shown in FIG. 6, and discussed in paragraph [0064], where these regions are described as being "buried" even though they are formed at the substrate surface, and are not covered by the substrate at their top surface. Thus, contrary to applicants' arguments, terms such as "buried" and "surrounding", as used in the semiconductor art, do not necessarily require that the region in question (i.e. bit lines) be completely enclosed and contacted at every point in three dimensional space by the substrate.

While applicants' inventive structure may indeed be novel, the present claim language fails to adequately distinguish this structure over the known prior art which also describes "buried" bit lines which are "surrounded" by substrate material.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Wojciechowicz whose telephone number is 571-272-1739. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edward Wojciechowicz
Primary Examiner